FORM PTO-1449 (Modified) U.S. Department of Commerce, Patent and Trademark Office					Docket No.		Serial No. W/676934		
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Twp	AR	Bothra, S., et al., "Integration of 0.25 µm Three and Five Level Interconnect System for High Performance ASIC", 1997 Proceedings Fourteenth International VMIC Conference, Santa Clara, CA, June 10-12, 1997, pp.43-48.							
TWP TWP	AS	Brongersma, S.H., et al., 'Non-Correlated Behavior of Sheet Resistance and Stress During Self-Annealing of Electroplated Copper", <u>IITC</u> , 1999, pp.290-292.							
ENP	Dobson, C.D., et al., "Advanced SiO ₂ Planarization Using Silane and H ₂ O ₂ ", Semiconductor International, December 1994, pp. 85-88.								
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.									

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-cup	BR	Universit	Hau-Riege, Stefan P., Handbook entitled "Copper Interconnect Technology", University of California-Berkeley Extension Course, April, 2002, pp. 129-137.							
TUP	BS	Kittel, Cha John Wile	Kittel, Charles, <u>Introduction to Solid State Physics</u> , 6th ed., New York: John Wiley & Sons, 1986, pp. 143, 145.							
Twp	ВТ	McClatchie, S., et al., "Low Dielectric Constant Oxide Films Deposited Using CVD Techniques", 1998 Proceedings Fourth International DUMIC Conference, February 16-17, 1998, pp. 311-318.								
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TUP	CR	Peters, Laura, "Low-k Dielectrics: Will Spin-On or CVD Prevail?", <u>Semiconductor International</u> , Vol. 23, No. 6, June, 2000, pp. 108-110, 114, 116, 118, 122, and 124.							
110(7)	cs	Peters, Laura, "Pursuing the Perfect Low-k Dielectric", <u>Semiconductor</u> <u>International</u> , Vol. 21, No. 10, September, 1998, pp. 64-66, 68, 70, 72, and 74.							
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